Docket No. A1WI2376US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Douglas W. Babcock, Robert A. Duris, Bruce Hecht

Serial No. 10/722,970

Filed: November 25, 2003

Title: AUTOMATIC TEST EQUIPMENT PIN CHANNEL WITH T- COIL COMPENSATION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF BRUCE HECHT

I, Bruce Hecht, declare:

1. I am a co-inventor of the invention which is the subject of the above-identified patent application.

2. At all times mentioned herein I was, and am presently a Staff Engineer for Analog Devices, Inc. (ADI), the assignee of the invention and patent application.

3. I have reviewed U.S. Patent No. 6,463,395 to Iorga, which has been cited in the above application. I understand inductance elements 97 and 99 in Fig. 7 of the patent to represent the inductances of the signal lead branches 91 and 93, respectively, in Fig. 6. Similarly, I understand the inductance elements 27, 29 in Fig. 2 to represent the inductances of signal lead branches 21, 23 in Fig. 1. My understanding of the patent is that equivalent inductances 97 and 99 are not coupled to each other, nor

are equivalent inductances 27 and 29. By contrast, the T-coil circuit disclosed in the above patent application includes a pair of coupled inductors L1 and L2. The coupling between these inductors is indicated at page 6, lines 1-2 of the application as follows: "These inductors are also coupled to one another by some degree of mutual inductance."; and at page 7, lines 3-6: "As indicated by the dotting convention used in the figures, the individual coils of each T-coil circuit are connected in series. The coils are also fabricated in proximity to each other so that they mutually couple."

4. On February 5, 2007 I conducted a series of circuit simulations, using the popular SPICE (Simulation Program with Integrated Circuit Emphasis) analog circuit simulator to compare the effectiveness of uncoupled vs. coupled inductors in compensating for load capacitance of 1pF, for a 500mV input with rise and fall times (between 10% and 90% of the step input) of 50ps. The circuits which I compensated are shown in attached Exhibit 1. The first circuit (circuit 0) drove a signal into a capacitive load, designated cload, in parallel with a resistive load, with no compensation. The next circuit (circuit 1) added two uncoupled compensation inductors on either side of the capacitive load, as in the Iorga patent. The next circuit (circuit 2) added to the uncompensated circuit 0 a pair of coupled inductors on either side of the load capacitor, connected as a T-coil with a coupling factor of 0.5. The last circuit (circuit 3) added a bridging capacitor to the T-coil, as in Figs. 1-3 of my patent application.

5. Exhibit 2 displays the responses of the four simulated circuits to an incident 1 volt step input with a 50 ohm source impedance, which caused a 500mv step at the Time-domain reflectometry (TDR) measurement point. A reflection "bump" was noted at approximately 11 nano seconds with each circuit. Simulations were performed for eight different conductor values, ranging from 0.25nH to 2.0nH in 0.25nH steps. Blow-ups of the reflection bump for circuits 0, 1, 2 and 3 are shown in Exhibits 3, 4, 5 and 6, respectively.

6. A "negative" reflection bump (below the 500mV step) is generally less desirable than a "positive" bump (above the 500 mV step) because it can cause false triggering in an automatic test equipment (ATE) system by causing the response to fall below the trigger threshold, which is typically 80% of the normal response from a device under test (DUT). A positive reflection bump can cause distortion, but this is normally more preferable than false triggers resulting from negative bumps.

7. In my simulated test, circuit 0 exhibited a negative bump of about 180mV (Exhibit 3). The Iorga-type compensation with uncoupled inductors exhibited a positive bump, followed by a negative bump and then a second positive bump before converging to the 500mV step level for all tested values of inductance (Exhibit 4). The responses ranged from a very slight positive peak and a negative peak of about -157mV for 0.25nH compensation inductors, to a positive peak of about 110mV and a negative peak of about -55mV for the maximum compensation of 2nH inductors. The

peak-to-peak difference between positive and negative excursions was on the order of 160mV in all cases.

8. With coupled compensation inductors (circuit 2), the reflection bump varied from almost all negative for 0.25nH inductors, to all positive for 1.25nH inductors and above (Exhibit 5). The peak-to-peak excursions ranged from about 130mV for 0.25nH, to about 50mV for 1.0nH, to about 110mV for 2.0nH inductors. This represented a significant improvement over the uncoupled inductor case of Exhibit 4, since it allowed a total elimination of negative bumps along with a significant reduction in peak-to-peak values.

9. For circuit 3, with a bridged T-coil, an even greater improvement was noted (Exhibit 6). In this case only the 0.75nH and 1.0nH inductors produced both and negative and positive peaks. In one case, with 0.75nH inductors, the negative and positive peaks were about -17mV and 7mV, respectively, while with 1.0nH inductors the negative and positive peaks were about -5mV and 47mV, respectively.

10. Exhibit 7 show the results of a SPICE simulation I also performed to compare the response, to a 500mV step input as for Exhibits 2-6, of (a) the Iorga circuit shown in Fig. 5 of the '395 patent (upper trace), (b) the T-coil circuit illustrated in Fig. 1 of the above patent application, without the bridge capacitor Cb1 (middle trace), and (c) the T-coil circuit with the bridge capacitor (lower trace). The simulations were performed with the same values of compensating inductors as for

Exhibits 2 and 4-6, and the results were similar. As shown in Exhibit 7, the Iorga circuit did not allow for the elimination of negative bumps within the test inductor range, while the two T-coil circuits did. The minimum peak-to-peak excursion for the Iorga circuit was about 145mV for a 500mV step. The corresponding minimum peak-to-peak excursions were about 51mV and 23mV for the T-coil circuit without and with a bridge capacitor, respectively. Thus, the use of mutually coupled inductors was found to both enable the elimination of negative bumps present with the Iorga circuit, and to reduce the maximum voltage excursion, with a bridge capacitor further improving the load capacitance compensation.

11. Exhibit 8 is a copy of a project schedule dated July 15, 2000 for the AD53510, which is the name of the ADI product that incorporated the subject matter of the above patent application within its "Core". Activities on the schedule dated prior to July 15, 2000 are marked with a check to indicate that they were started and completed on the dates indicated; activities dated after July 15, 2000 show scheduled start and completion dates. I am the "Bruce" referred to on the "Design Review" line, and I was a member of the "Team" referred to below that.

12. The next to last entry on page 1 of Exhibit 8 refers to trimming, testing and shipping samples for Agilent, a customer of ADI for other products. The last entry on page 1, "MCM Assy by Tyco", refers to the fact that sample AD53510 dies were actually sent to Tyco, a subcontractor for Agilent, which assembled the dies into a

multi-chip module for Agilent. The first entry on page 2 of Exhibit 8, "Agilent Eval of MCM", refers to a characterization and evaluation of the dies on the multi-chip module that was performed by Agilent. Based upon Agilent's feedback to ADI, extensive modifications to the AD53510 design were afterwards made by ADI.

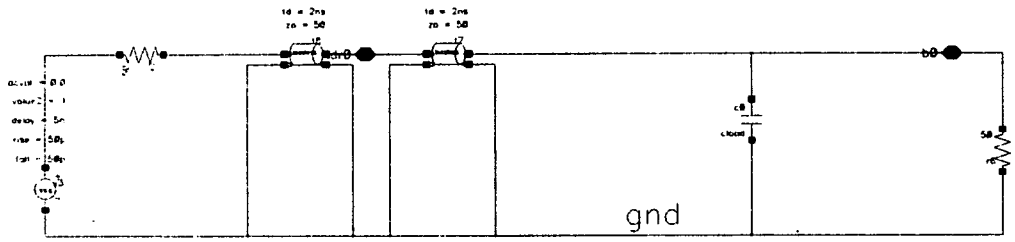
13. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: February 26, 2007 Bruce Hecht

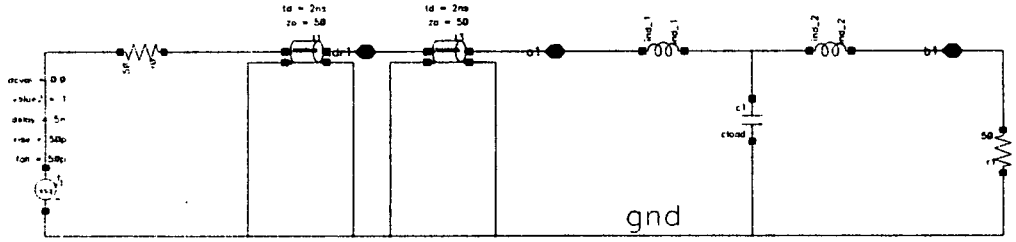
Bruce Hecht

(U:MR/RSK/Dec./D. of B. Hecht A1WI2376US)

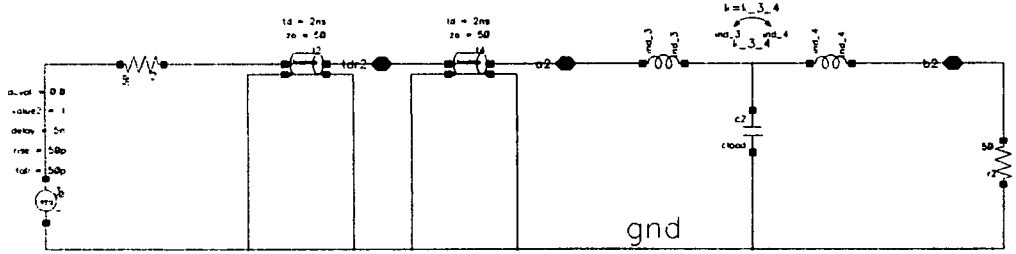
EXHIBIT 1 - HECHT



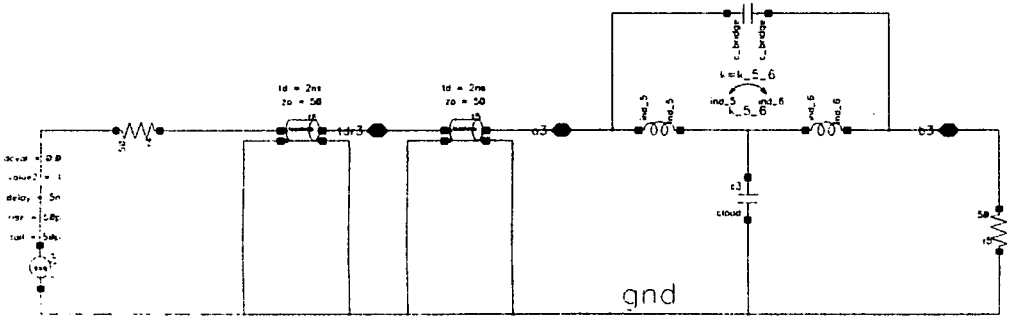
Circuit Ø
no compensation of CLOAD



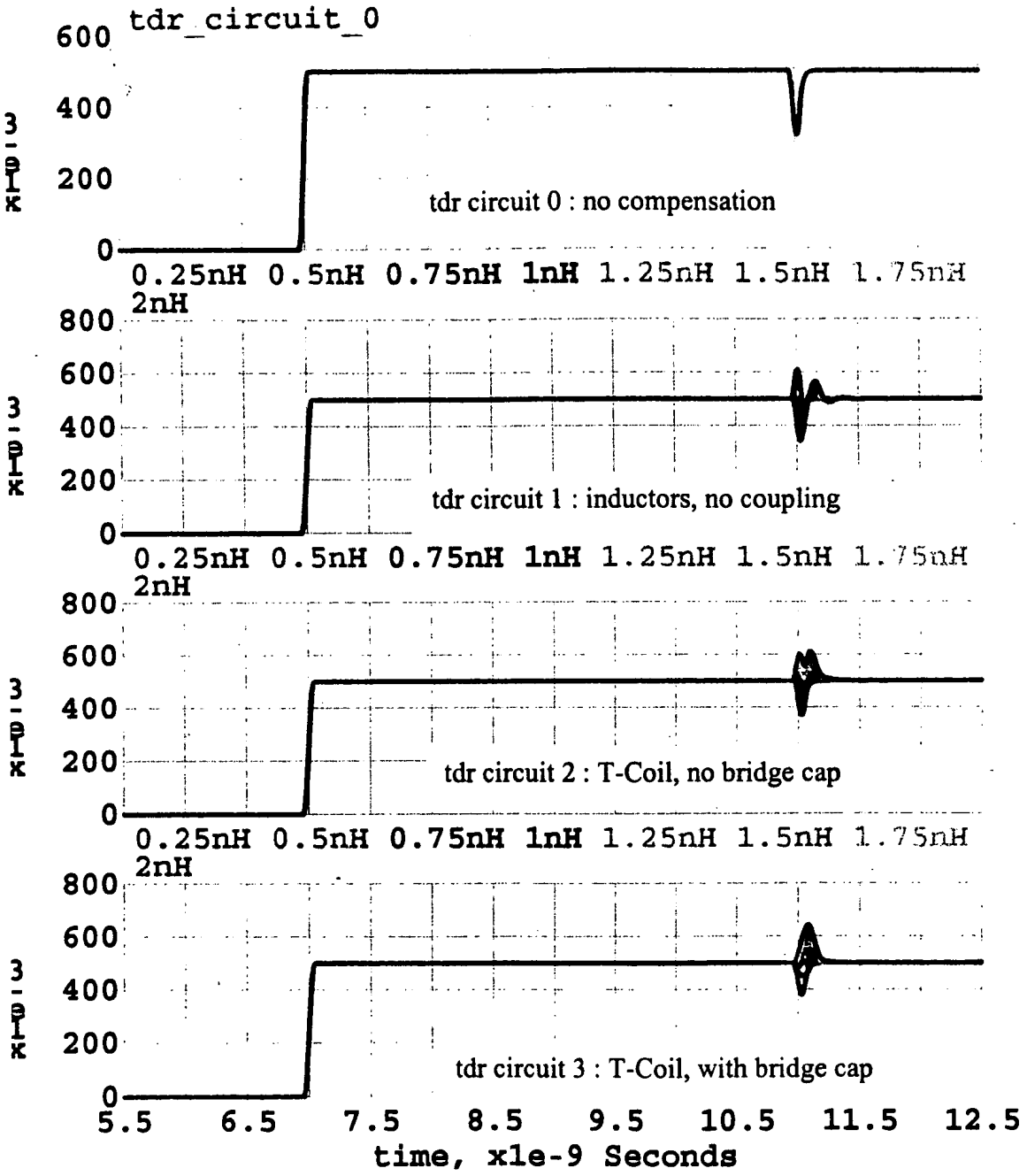
Circuit 1
Compensation of CLOAD
with inductors (not coupled)



Circuit 2
Compensation of CLOAD
with T-coil (coupled inductors)



Circuit 3
Compensation of CLOAD
with T-coil (coupled inductors)
with bridging capacitor


tdr_circuit_0
600
400
200
0
3-pin
tdr circuit 0 : no compensation
0.25nH 0.5nH 0.75nH 1nH 1.25nH 1.5nH 1.75nH 2nH
800
600
400
200
0
3-pin
tdr circuit 1 : inductors, no coupling
0.25nH 0.5nH 0.75nH 1nH 1.25nH 1.5nH 1.75nH 2nH
800
600
400
200
0
3-pin
tdr circuit 2 : T-Coil, no bridge cap
0.25nH 0.5nH 0.75nH 1nH 1.25nH 1.5nH 1.75nH 2nH
800
600
400
200
0
3-pin
tdr circuit 3 : T-Coil, with bridge cap
5.5 6.5 7.5 8.5 9.5 10.5 11.5 12.5
time, x1e-9 Seconds

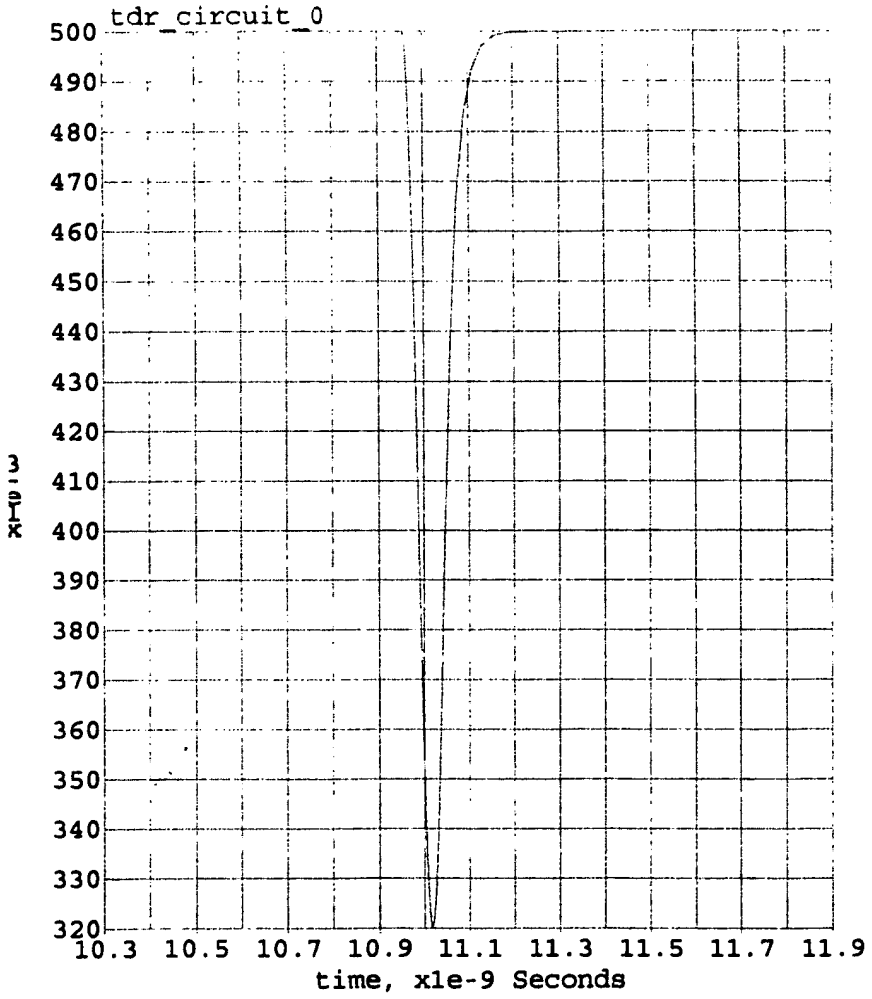


EXHIBIT 3 - HECHT

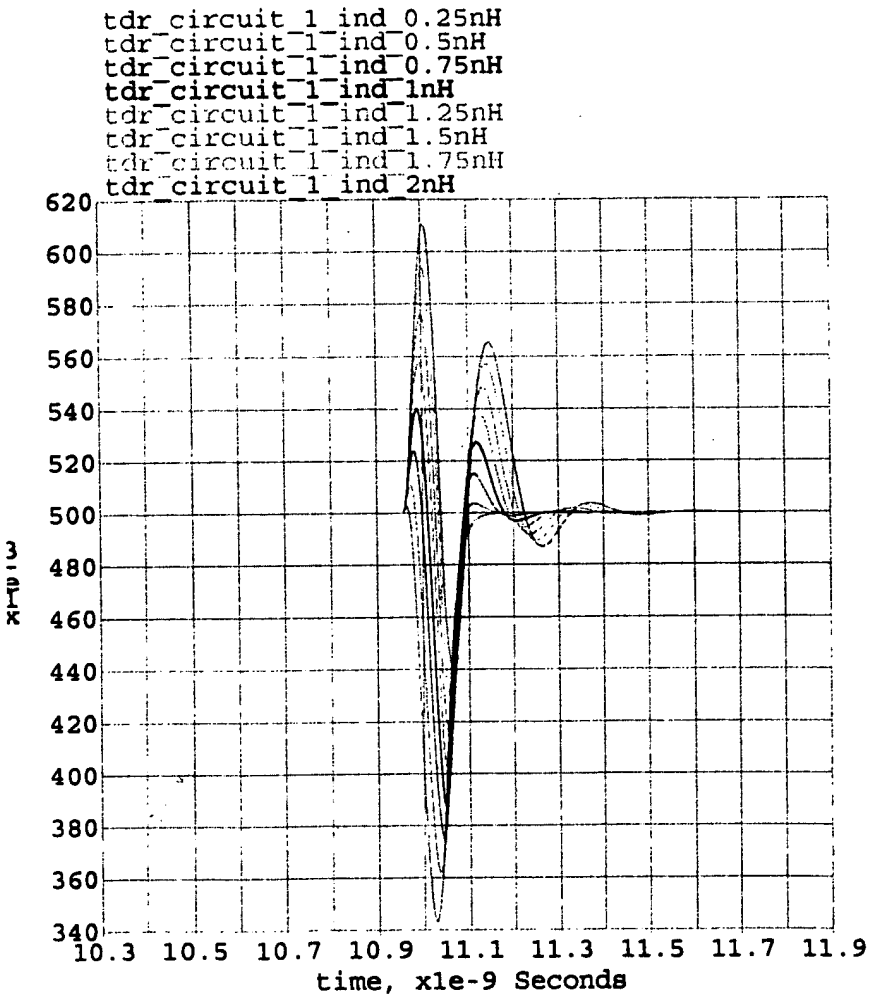


EXHIBIT 4 - HECHT

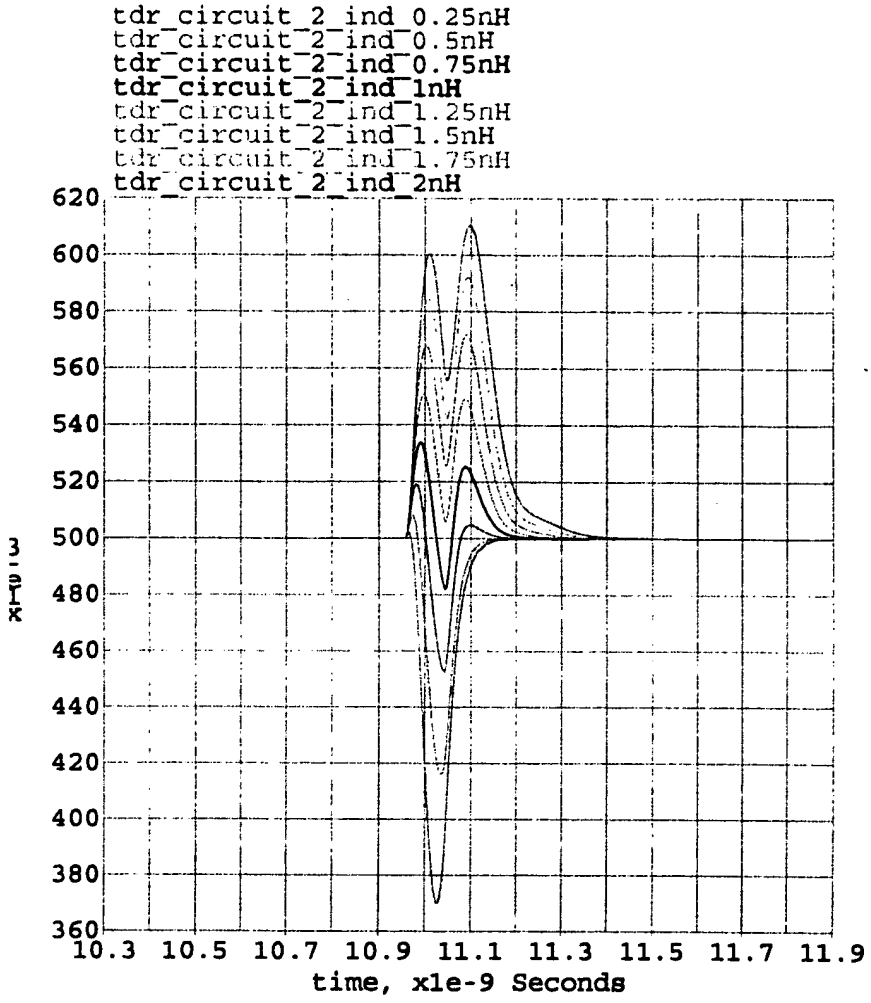


EXHIBIT 5 - HECHT

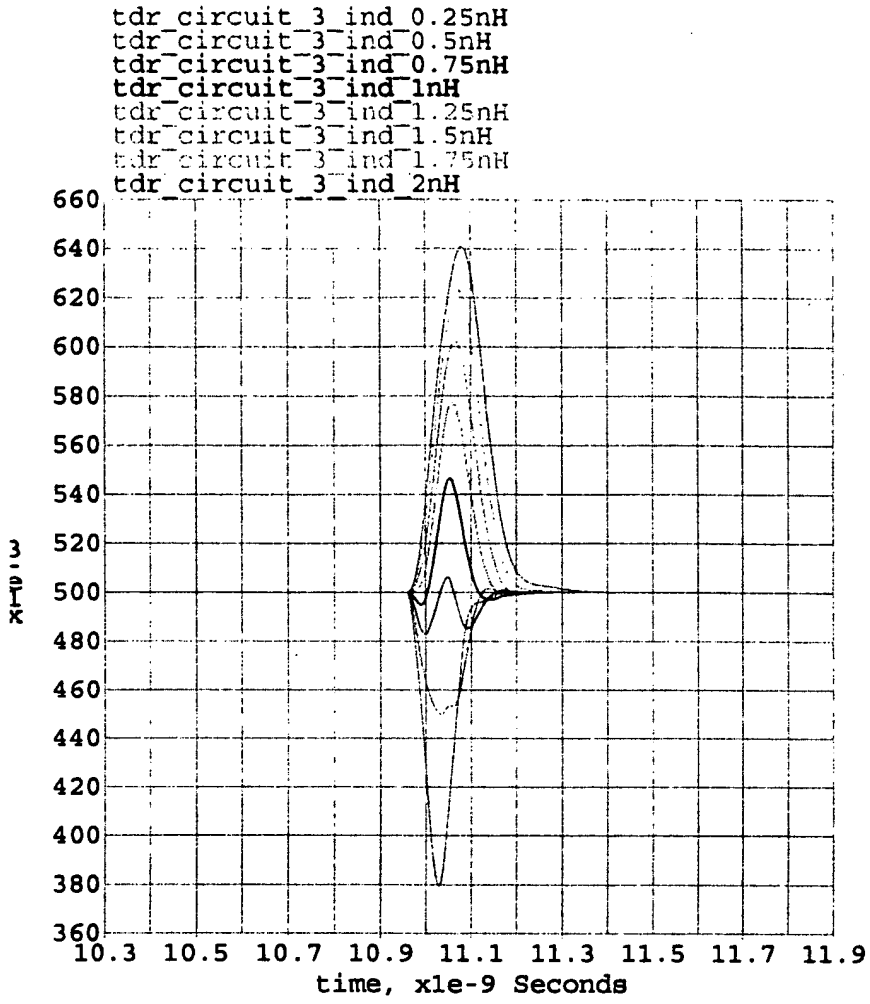
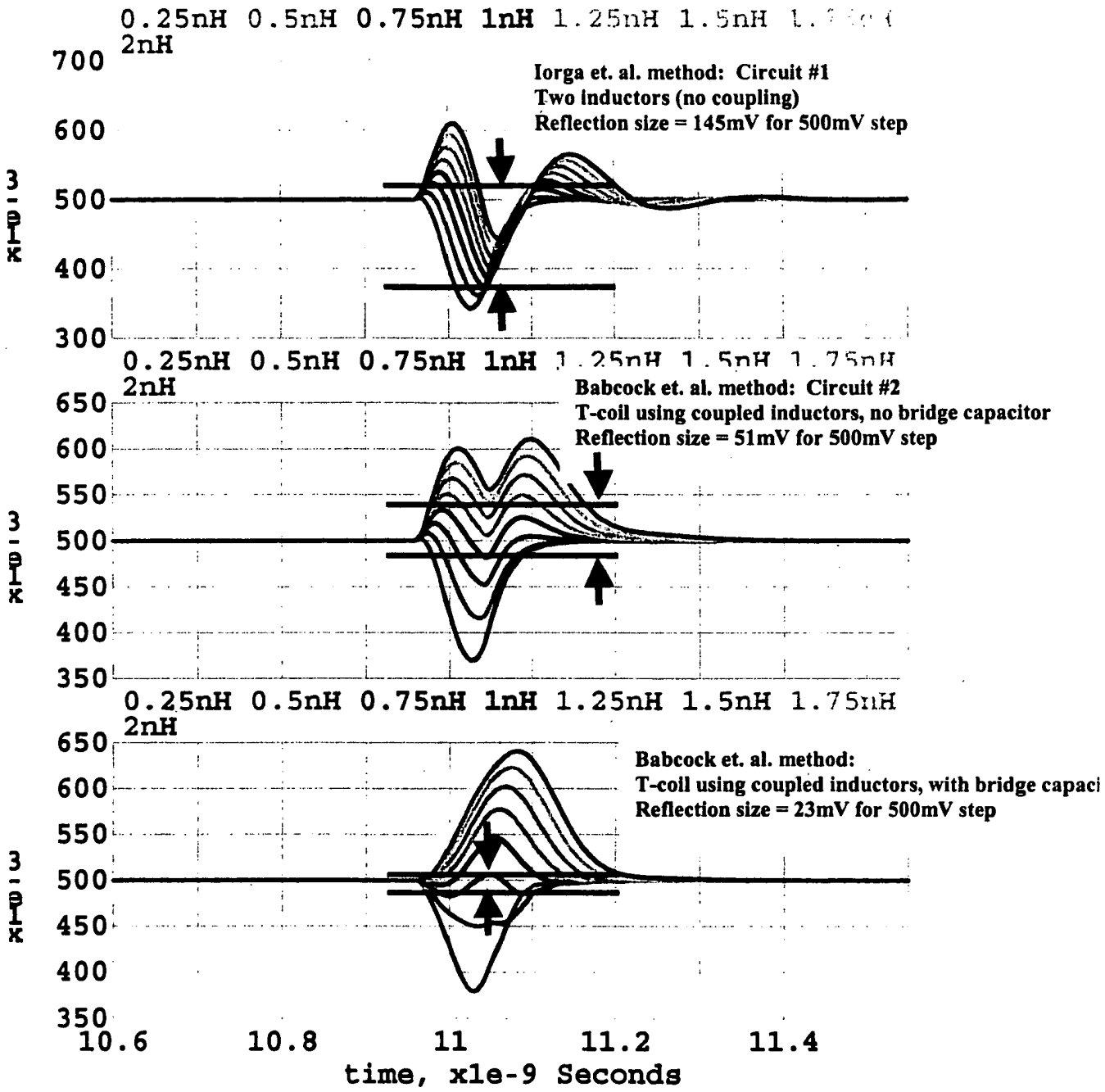
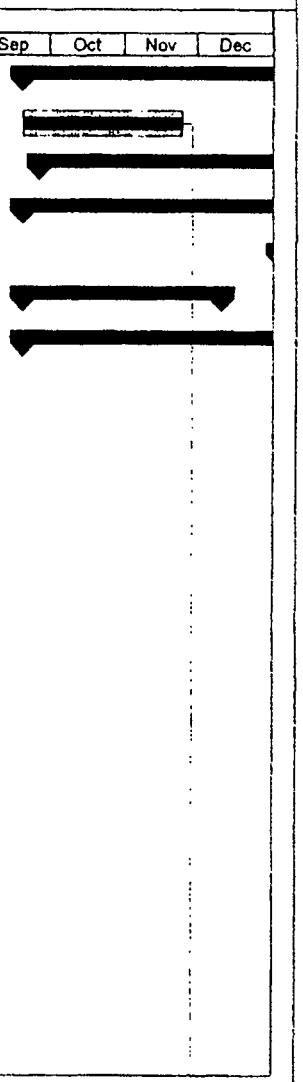


EXHIBIT 6 - HECHT


0.25nH 0.5nH 0.75nH 1nH 1.25nH 1.5nH
2nH
Iorga et. al. method: Circuit #1
Two inductors (no coupling)
Reflection size = 145mV for 500mV step
700
600
500
400
300
0.25nH 0.5nH 0.75nH 1nH 1.25nH 1.5nH 1.75nH
2nH
Babcock et. al. method: Circuit #2
T-coil using coupled inductors, no bridge capacitor
Reflection size = 51mV for 500mV step
650
600
550
500
450
400
350
0.25nH 0.5nH 0.75nH 1nH 1.25nH 1.5nH 1.75nH
2nH
Babcock et. al. method:
T-coil using coupled inductors, with bridge capaci
Reflection size = 23mV for 500mV step
650
600
550
500
450
400
350
10.6
10.8
11
11.2
11.4
time, x1e-9 Seconds

AD53510 XFCB2.0 Dual Driver / Comparator / Formatter
Project Schedule - July 12, 2000

ID	% Con		Task Name	Duration	Start	Finish	Predeces	Resource Nan
25	48%		**Core Development**	**302 days**	**Mon 9/20/99**	**Wed 11/29/00**		**Team**
26	100%	✓	Formatter/AB delays due to conflicts	9 wks	Mon 9/20/99	Wed 11/24/99		
27	100%	✓	**Driver Design**	**104 days**	**Mon 9/27/99**	**Fri 3/3/00**		
35	100%	✓	**Formatter Design**	**92.81 days**	**Mon 9/20/99**	**Thu 2/10/00**		
44	100%	✓	**Miscellaneous Cells**	**15 days**	**Mon 1/3/00**	**Mon 1/24/00**		
48	100%	✓	**Comparator Design**	**55 days**	**Mon 9/20/99**	**Fri 12/10/99**		
52	100%	✓	**AB Driver Design**	**96 days**	**Mon 9/20/99**	**Tue 2/15/00**		
58	100%	✓	Top Level (Class A layout complete by 3/24)	2 wks	Wed 1/19/00	Fri 2/25/00	57	Ken S./Bob D.
59	100%	✓	Design Review	1 day	Mon 2/28/00	Mon 2/28/00	58	Bob,Doug,Bru
60	100%	✓	Layout Review	1 day	Tue 2/29/00	Tue 2/29/00	59	Jack,Ray
61	100%	✓	Top Level Simulations	17 days	Wed 3/1/00	Thu 3/23/00	60	Team
62	100%	✓	Power reduction design (Logic, IO, Comp Pwr Dn)	3 days	Fri 3/24/00	Tue 3/28/00	61	Team
63	100%	✓	Final pwr reduction/top level layout	17 days	Wed 3/29/00	Thu 4/20/00	62	Team
64	100%	✓	Final top level simulations	5 days	Fri 4/21/00	Thu 4/27/00	63	Team
65	100%	✓	Final Design Review	1 day	Fri 4/28/00	Fri 4/28/00	64	Team
66	100%	✓	Tape out	20 days	Mon 5/1/00	Fri 5/26/00	65	Jack
67	50%		Wafer Fab	10.6 wks	Mon 5/29/00	Wed 8/9/00	66	
68	0%		Trim first samples with Met3 T-Coil	5 days	Tue 8/22/00	Mon 8/28/00	67,131	
69	0%		Ship Met3 T-coil samples to Agilent	1 day	Tue 8/29/00	Tue 8/29/00	68	
70	0%		T-Coil Fab (post process) AMS	4 wks	Thu 8/10/00	Wed 9/6/00	67	
71	0%		T-Coil Fab (post process) MEMSCAP	4 wks	Thu 8/10/00	Wed 9/6/00	67	
72	0%		Trim, Test and ship Func T-coil Samples for Agilent	2 wks	Thu 9/7/00	Wed 9/20/00	71	
73	0%		MCM Assy by Tyco	2 wks	Thu 9/21/00	Wed 10/4/00	72	John Dixon



Project: AD53510_Schedule_Rev0
Date: Mon 7/17/00

Task
Split
Progress
Milestone
Summary
Rolled Up Task
Rolled Up Split
Rolled Up Milestone
Rolled Up Progress
External Tasks
Project Summary

EXHIBIT 8, p. 1 - HECHT

AD53510 XFCB2.0 Dual Driver / Comparator / Formatter
Project Schedule - July 12, 2000

ID	% Con	O	Task Name	Duration	Start	Finish	Predeces	Resource Nan
74	0%		Agilent Eval of MCM	4 wks	Thu 10/5/00	Wed 11/1/00	73	

Aug | Sep | Oct | Nov | Dec

Project: AD53510_Schedule_Rev0
Date: Mon 7/17/00

Task | Split | Progress | Milestone | Summary | Rolled Up Task | Rolled Up Split | Rolled Up Milestone | Rolled Up Progress | External Tasks | Project Summary

EXHIBIT 8, p. 2 - HECHT